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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,403	01/26/2004	Ho-young Song	5649-1180	2218

20792 7590 07/26/2006

MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,403	SONG, HO-YOUNG	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4-24-2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,20-27,29-40 and 43-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-8,10-11,13-14,20-27,29-35,38,40 and 45* is/are allowed.

6)☒ Claim(s) *1-6, 9, 12, 36-37, 39 and 43* is/are rejected.

7)☒ Claim(s) *44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10-19-2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of the Amendment filed 4-24-2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 36 and 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Braceras et al. (US PAT No. 6,501,293).

Regarding claim 1, Fig. 7 of Braceras et al. teaches a termination transistor for a transmission line for a transmission line (active termination; col. 5, lines 26-50), the termination transistor comprising: an input node (SIGNAL_PAD2) receiving an input signal (signal from CPU) over the transmission line (706); an NMOS pull-down transistor (N0) coupled between the input node and a first reference voltage (Ground) wherein the NMOS pull-down transistor is configured to provide an electrical path (path from the node to the Ground) between the first reference voltage and the input node responsive to the input signal having a first voltage level (when input signal at the node is logic high, N0 is turned); and a PMOS pull-up transistor (P0) coupled between the input node (SIGNAL_PAD2) and a second reference voltage (VDDQ) wherein the PMOS pull-up transistor is configured to provide an electrical path (path from the node to VDDQ)

between the second reference voltage and the input node responsive to the input signal having a second voltage level (when input signal at the node is logic low, P0 is turned), wherein the first reference voltage is less than the second reference voltage (Ground is less than VDDQ) and wherein the first voltage level is greater than the second voltage level (logic high is greater than logic low) wherein the NMOS pull-down transistor maintains the electrical path between the first reference voltage and the input node while the input signal is maintained steady state at the first voltage level (as long as the input signal at the node is logic high, N0 remains to be turned on); wherein the PMOS pull-up transistor maintains the electrical path between the second reference voltage and the input node while the input signal is maintained steady state at the second voltage level (as long as the input signal at the node is logic low, P0 remains to be turned on).

Regarding claim 2, Fig. 7 of Braceras et al. teaches a termination transistor according to claim 1 wherein the first voltage level comprises a logic high voltage level (the voltage turns on NMOS is the logic high level) and wherein the second voltage level comprises a logic low voltage level (the voltage turns on PMOS is the logic low level).

Regarding claim 3, Fig. 7 of Braceras et al. teaches a termination transistor according to claim 1 wherein the first reference voltage comprises a ground voltage (N0 is coupled to ground) and the second reference voltage comprises a supply voltage (VDDQ is the supply voltage).

Regarding claim 4, Fig. 7 of Braceras et al. teaches a termination transistor according to claim 1 wherein: the NMOS pull-down transistor is further configured to block the electrical path between the first reference voltage and the input node responsive to the input signal having the second voltage level (when the input voltage at the node is logic low, N0 is turned off and blocks the path between the ground and the node; and the PMOS pull-up transistor is further configured to block the electrical current path between the second reference voltage and the input node responsive to the input signal having the first voltage level (when the input voltage at the is logic high, P0 is turned off and blocks the path between the VDDQ and the input node).

Regarding claim 5, Fig. 7 of Braceras et al. teaches a termination transistor according to claim 4 wherein the NMOS pull-down and the PMOS pull-up transistor are further configured to provide electrical paths between the input node and both of the first and second reference voltages at a same time during a transition of the input signal between the first and second voltage levels (during the input signal transition from logic low to logic high or vice versa, P0 and N0 are turned on at the same time which is a leakage current, and the leakage current is inherently present in the CMOS structure comprising of PMOS and NMOS).

Regarding claim 36, Fig. 7 of Braceras et al. teaches a termination transistor which reduces ringing and dynamic current (col. 5, lines 26-67), which occur when an

input signal is transmitted through a transmission line to an input node (SIGNAL_PAD2 coupled to transmission line 706), the termination transistor comprising: a pull-down unit including an NMOS pull-down transistor (N0) which prevents a voltage level at the input node from reaching a voltage level of a second voltage (VDDQ) when a voltage level of the input signal at the input node is at a first level (logic high level, e.g. when input signal at the node is logic high, N0 is turned on and pulls the node to ground preventing the node rising to VDDQ); and a pull-up unit including a PMOS pull-up transistor (P0) which prevents a voltage level at the input node from reaching a voltage level of a first voltage (ground) when a voltage level of the input signal at the input node is at a second level (logic low, e.g. when input signal at the node is logic low, P0 is turned on and pulls up the node to VDDQ preventing the node being pulled down to ground), where a voltage level of the first voltage (logic low) is the same as a voltage level of a ground voltage (ground) and a voltage level of the second voltage (logic high) is the same as a voltage level of a supply voltage (VDDQ) where the first level (logic high) is high and the second level (logic low) is low.

Regarding claim 43, Fig. 7 of Braceras et al. teaches the termination transistor of claim 36, wherein the termination transistor is mounted in a semiconductor chip (active termination circuit can be located in CPU or memory; col. 5, lines 40-42).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6, 9, 12 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Braceras et al. in view of Volk (US PAT No. 6,356,105).

Regarding claim 6, 9, 12 and 37-39, Braceras et al. teaches a termination transistor according to claims 1 and 36 where the transistors P0 and N0 provides active terminations, but does not teach a pull-down resistor in series with the NMOS pull down transistor nor a pull-up resistor in series with PMOS pull up transistor. However, Fig. 5 of Volk teaches a pull-down resistor (R2) in series with NMOS transistor (N1) between the input node and the first reference voltage and a pull-up resistor (R1) in series with PMOS transistor (P1) between the input node and the second reference voltage for the purpose of compensating difference in Ptype and Ntype transistors (col. 7, lines 35-41). It would have been obvious at the time of invention to include additional pull-down and pull-up resistors in series with PMOS and NMOS in order to provide balanced and improved termination.

Allowable Subject Matter

Claims 7-8, 10-11, 13-14, 20-27, 29-35, 38, 40 and 45 are allowable over the prior art of record.

Claim 44 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to teach, among other things, the specific of a first input resistor coupled between the input node and a gate electrode of the NMOS transistor and a second input resistor coupled between the input node and a gate electrode of the PMOS transistor.

Response to Arguments

Applicant's arguments with respect to claims 1-6, 9, 12, 36-37, 39 and 43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

James Cho
Primary Examiner
Art Unit 2819